Three tracking scenarios for sPHENIX

Tony Frawley

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sPHENIX tracking requirements

Maximum (instantaneous) collision rates:

- Au+Au 100 kHz
- p+p 12 MHz

Momentum resolution:

- Δ pT/pT < 1.2% for pT < 10 GeV/c
- Depends on tracker radius and tracker mass

Efficiency and pattern recognition:

- Track reconstruction efficiency > 90% at I GeV/c, ~ 98% at pT > 2 GeV/c
- Fake rate < a few per 5000 Hijing events

The purpose of these slides is to outline three possible tracking scenarios that may be able to deliver this performance.

Functionality

The tracker is best thought of as having two parts:

 Both parts should be as thin as possible to minimize radiative energy loss, regardless of momentum resolution considerations

Inner tracker

- Displaced vertex measurement (driven by B, D jet physics)
- Pattern recognition and matching to the outer tracker

Outer tracker:

- Momentum measurement (driven by Upsilon physics)
- Pattern recognition

To a considerable degree the choice of inner tracker can be separated from the choice of outer tracker

Inner tracker

Inner tracker

- Displaced vertex measurement (driven by B jets physics)
- Pattern recognition and matching to the outer tracker

General remarks:

- Prefer three pixel layers for redundancy in displaced vertex measurement
- May need additional layer(s) for good matching to outer tracker
 - Not necessarily pixels

Possibilities:

- ALICE ITS upgrade
- LANL LDRD
- Re-use PHENIX pixels

Re-using the PHENIX pixels has two undesirable features:

- Only two layers
- Both layers have significant dead areas

And a desirable feature:

Low cost!

Outer tracker

Outer tracker:

- Momentum measurement (driven by Upsilon physics)
- Pattern recognition

General remarks:

- Momentum resolution for Upsilon determined primarily by tracking radius and mass of material
- Momentum resolution at high p_T better for silicon, but it does not matter for any any physics?
- Pattern recognition determined by the number and configuration of layers

Possibilities:

- ALICE ITS upgrade
- TPC
- New Si strip layers

Possible building blocks

ALICE ITS upgrade detector

All layers composed of pixels.

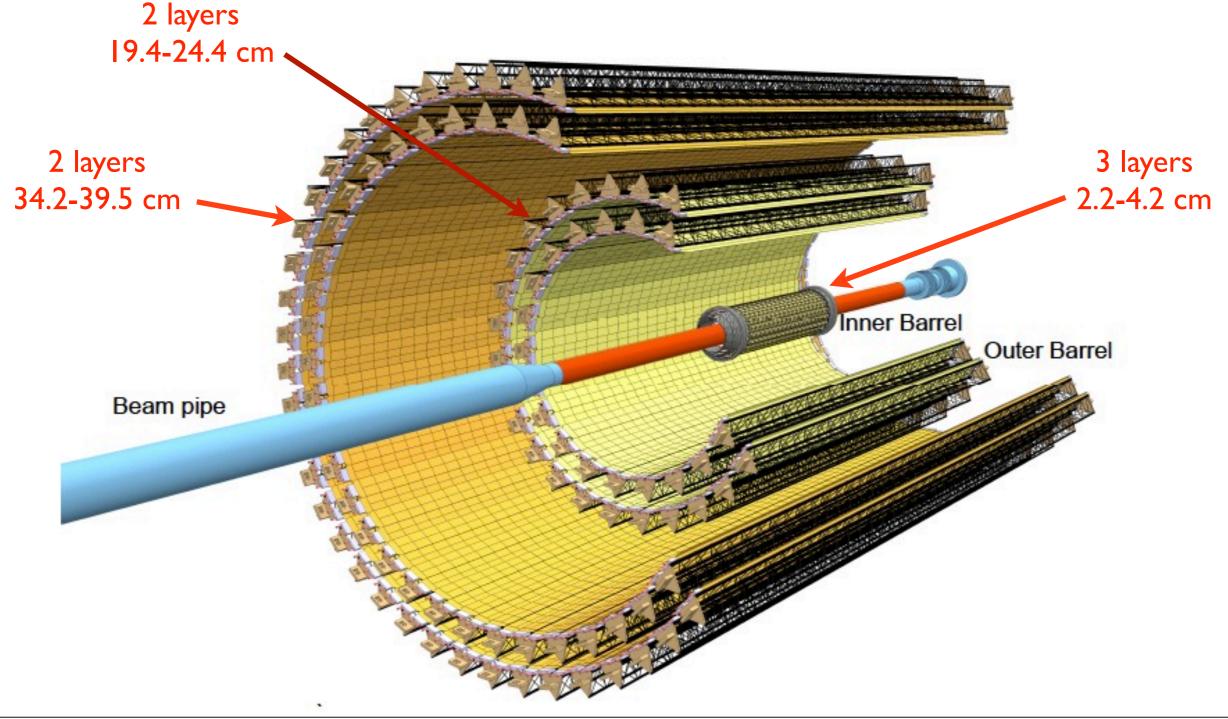
• Inner three layers: 0.3% / layer

• Outer four layers: 0.8% / layer

Total thickness $X/X_0 = 4.1\%$

Pixel sizes: inner barrel 20-30 x 20-30 μm

outer barrel 20-50 x 20-50 μm



LANL LDRD detector

Pre-proposal by Mike McCumber

- Aimed at low mass inner tracker for displaced vertex measurement
- Driven by B, D jet physics requirements
- Three layers of pixels
- Low mass

Details are not well defined yet

Will include intermediate layer(s) for track matching to outer tracker?

Reconfigured PHENIX pixels

Two layers of pixels Radius 2.7 cm and 4.6 cm pixel size 50 µm x 425 µm

Significant dead areas in both layers

Mass 1.3% X₀ per layer Total mass 2.6% X₀

New Si strip detector

Proposal by Yasuyuki Akiba

- Si strip tracker using 320 µm thick sensors
- Strip pitch 60 μm
- Z segmentation 8 mm or 16 mm
- 5 layers covering 9.5 cm to 80 cm radius

Proposed readout: SVX4 chip

Objections to SVX4:

- Can not mount enough SVX4 chips to read out all strips
 - One dead channel removes multiple strips
 - pattern recognition is adversely affected
- High power consumption
- Not compatible with very low mass detector

Should consider different readout chip

- Higher density so can read out all strips
- lower power consumption
- lower mass

TPC

GEM readout TPC

- Inner radius 40 cm
- Outer radius 80 cm

Gas (based on ILC prototype measurements)

- Ar(95%) CF4(3%) Isobutane(2%)
- $N_t = 38$ electrons/keV
- $V_{drift} = 6 \text{ cm/}\mu\text{s}$ at $\sim 150 \text{ V/cm}$
- $D_t = 57 \,\mu\text{m}/\sqrt{\text{cm}}$ in 1.45 T field
- $W_t = 2.2$
- $X_0 = 11633$ cm

Charge sharing between 2-3 pads of 1.2 mm (ILC prototype measurements)

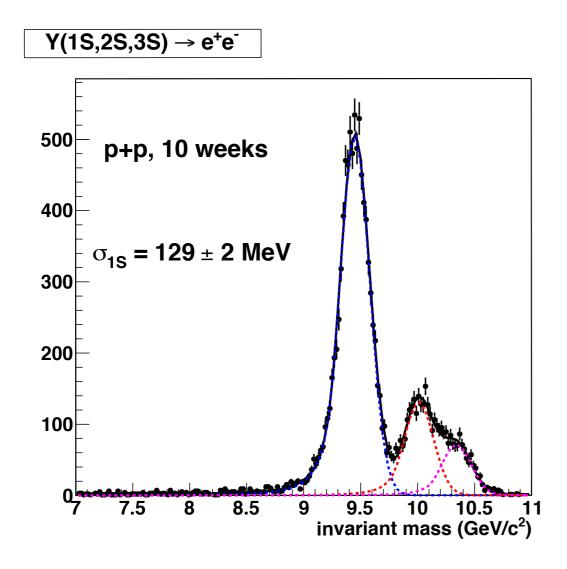
- σ_{charge} = 300 μm in triple GEM
- $\sigma_0 = 70-80 \ \mu m$

Scenario I

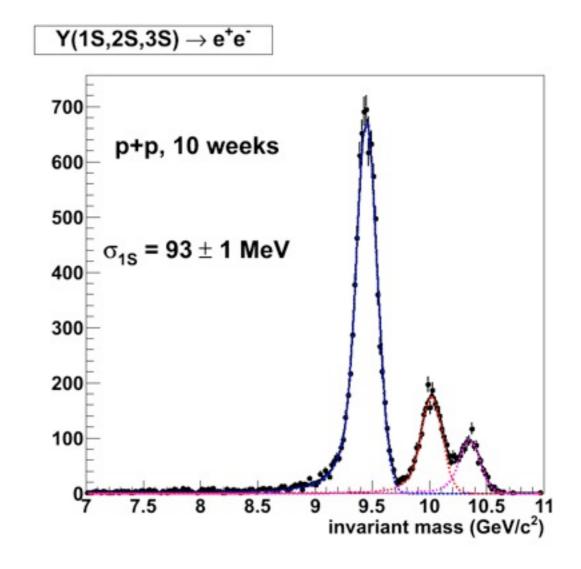
Scenario I - ITS inner tracker (all layers)

Need to stretch radius to meet our momentum resolution spec. Consider 20x20 and 20x20 µm pixel size Total thickness = 4.1%

Outer radius **40 cm** mass resolution not good enough



Outer radius **60 cm** mass resolution better than spec

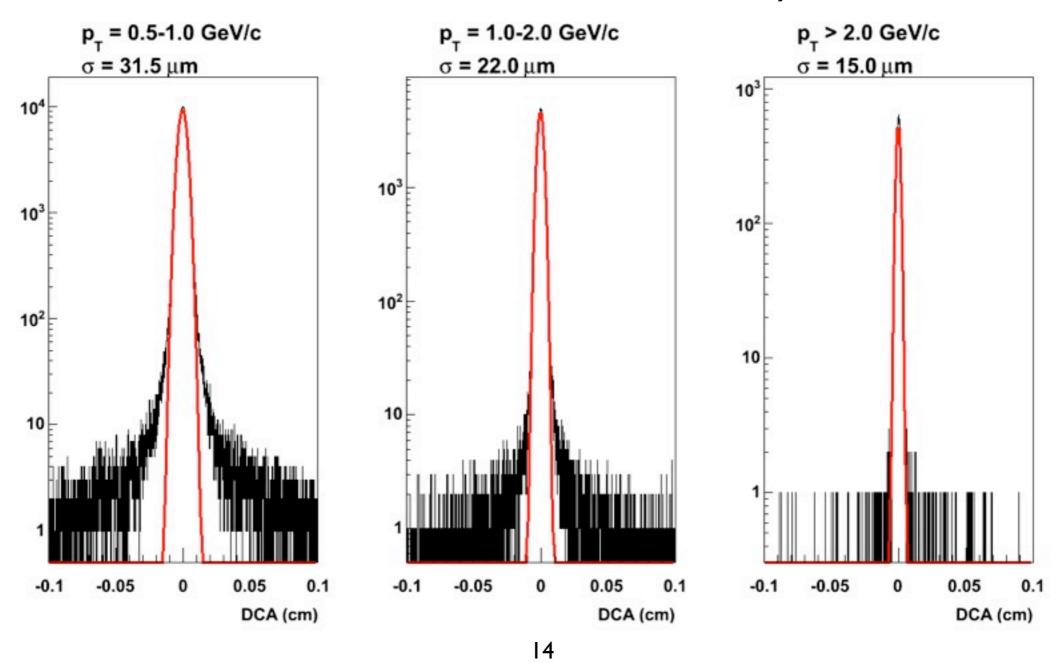


Scenario I - ITS inner tracker (all layers) (cont.)

Need to stretch radius to meet our momentum resolution spec Consider 20x20 and 20x20 μm pixel size

Total thickness = 4.1%

DCA resolution 60 cm outer layer



Scenario I - ITS inner tracker (all layers) (cont.)

Need to stretch radius to meet our momentum resolution spec Consider 20x20 and 20x20 µm pixel size Total thickness = 4.1%

Comments/Questions:

- Best possible resolution at outer tracker radius of 80 cm would be ~ 70 MeV
- Could meet our mass resolution spec of 100 MeV by setting outer tracker layer radius to about 55 cm
- Cost?

Pros:

- ITS development being done for ALICE
- Low technical risk

Cons:

- None for sPHENIX (besides probably cost)?
- Not reusable for EIC detector

Scenario I - Questions to be addressed by simulations

Use ITS first 5 layers (3 pixels + 2 intermediate layers)

- Place layers 6 and 7 at various trial radii (50, 55, 60, 65 cm)
- Evaluate performance with each trial radius for layers 6 and 7
 - DCA performance
 - Momentum resolution
 - Pattern recognition
 - Do the intermediate two layers have to be stretched too?
 - What is the maximum pixel size we could use?

Scenario 2

Scenario 2 - ITS layers I-5 + TPC

Total thickness 4%

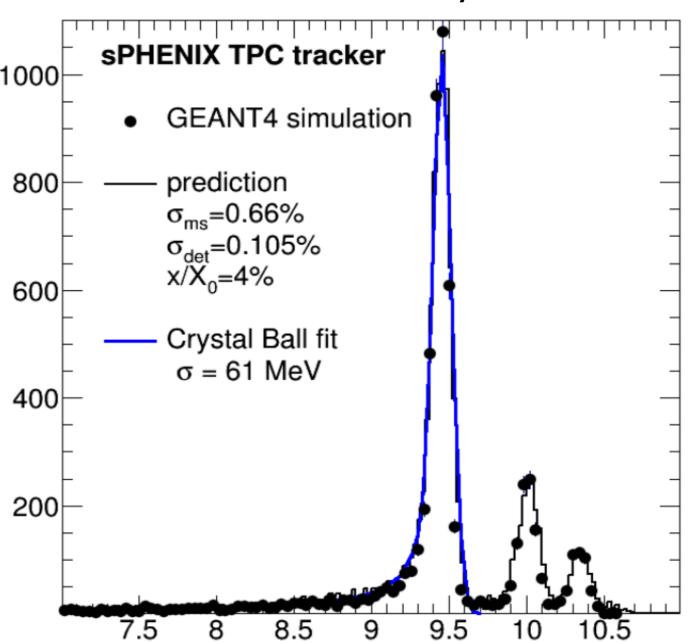
ITS:

- Inner barrel (3 pixel layers)
 First 2 layers of outer barrel • Inner barrel (3 pixel layers)
- Outer radius of 24.4 cm
- Thickness 2.5%

TPC

- radius 40 80 cm
- Thickness 1.34% (?)
 - Gas (40 cm) 0.34%
 - Field cage 1.0%

Performance should be very similar to this



Scenario 2 - ITS layers I-5 + TPC (cont.)

Total thickness 4%

Comments/questions:

- TPC space charge effects need to be modeled to show that detector can operate at 100 kHz Au+Au
- Cost of ITS layers 1-5?
- Cost of TPC?
- Cost reduction for TPC if outer radius reduced to give mass resolution of 100 MeV?
- Would track matching from ITS to TPC be good enough with only ITS layers 1-3?

Pros:

- ITS development done by ALICE
- TPC electronics would be reused in EIC detector
- Particle ID from TPC dE/dx?

Cons:

• Have to understand if space charge effects at very high rate are a problem

Scenario 2(a) - LANL LDRD detector + TPC

Total thickness ??

Performance presumably similar to ITS layers I-5 + TPC in performance.

Comments/questions:

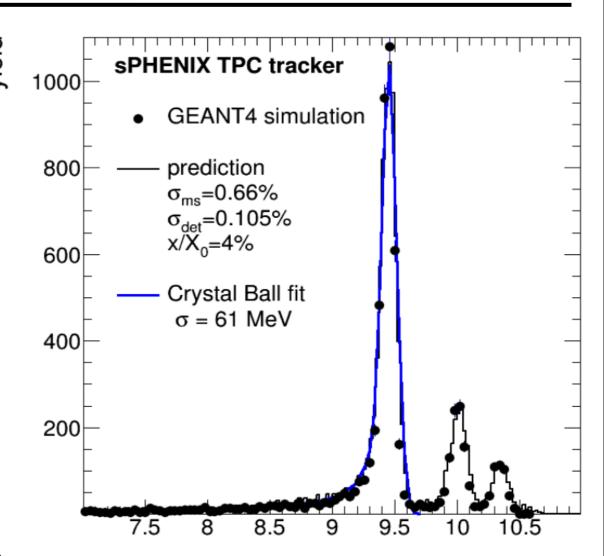
- Cost? Maybe cheaper than ITS inner layers?
- LDRD detector design will need to consider track matching to the TPC.

If a layer outside of the pixels is needed for track matching, needs to be understood how this would be made.

Scenario 2(b) - Reconfigured PHENIX pixels + TPC

Total thickness 4%

Momentum resolution 61 MeV for Upsilons



Comments/questions:

- Pixels will be cheap
- B physics impacted by dead areas, but doable
- Upsilon physics can probably use the OR of the two layers for tracking
- Will need to consider track matching to the TPC
- Can we match tracks in AuAu events without an intermediate layer?
 - If not, how do we get an intermediate layer?

Scenario 2 - questions to be addressed by simulations

Aside from understanding TPC high rate (space charge) performance, we need to understand - using G4 simulations - how to combine a displaced vertex detector and a TPC into our tracker:

- Start with 2 or 3 layers of pixels inside 6 cm or so
- Add TPC from 40 cm to max TPC radius
- Try tracking in central HIJING events
 - Good pattern recognition?
 - Explore changing outer TPC radius

As necessary, add intermediate Si layers in the 10-30 cm radial envelope until we get good pattern recognition

- For the ITS option this would be ITS layers 4 and 5
- For the LANL LDRD detector it would be part of the design (?)
- For the two reconfigured PHENIX pixel layers it would have to be a new detector

The TPC brings the option of particle ID by dE/dx

• What physics can we add with this?

Scenario 3

Scenario 3 - ALICE ITS (3 pixel layers) + outer Si strip tracker

Outer radius 65-70 cm (rough est.) needed to meet momentum resolution spec Total thickness 0.9% + 6.7% = 7.6%

ITS:

- Inner barrel (3 pixel layers)
- Thickness 0.9%

Si Strip tracker:

- radius 9.5 80 cm
- Thickness 6.7%

This just replaces the two layers of reconfigured PHENIX pixels in the reference design with three layers of state of the art, low mass pixels

Reduces the total mass by 1.7% and will improve the displaced vertex measurement. Also, three pixel layers will add considerable robustness to the tracking.

Scenario 3 - ALICE ITS (3 pixel layers) + outer Si strip tracker

Outer radius 65-70 cm (rough est.) needed to meet momentum resolution spec Total thickness 0.9% + 6.7% = 7.6%

Comments/questions on outer tracker:

- What chip should be used? We want:
 - low power/low mass
 - Dense enough to read out all channels
- Can we use stereo layers to increase redundancy, keep good pattern recognition?
- How thin can the support structure/cooling be made?
 - Trade off with outer radius
 - Reduced radiative tails
 - Depends on power consumption
- Cost?

Pros:

performance simulated already

Cons:

Large mass (as is)
Requires a lot of engineering
Need to settle issues outlined above

Scenario 3 (a) - LANL LDRD detector + outer Si strip tracker

Outer radius 65-70 cm needed to meet momentum resolution spec Total thickness ?? + 6.7%

Performance presumably similar to ITS inner barrel + Si strip tracker

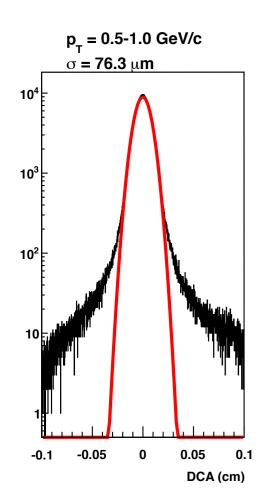
Questions/comments:

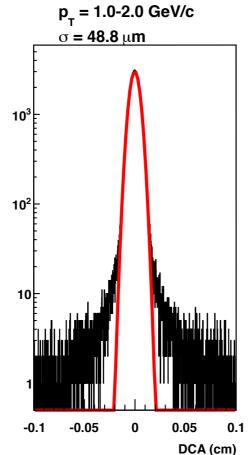
Cost smaller than ALICE ITS inner barrel? Thickness?

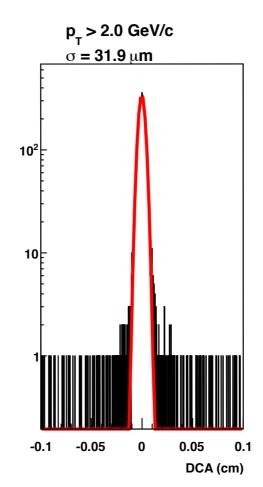
Scenario 3 (b) - PHENIX pixels + outer Si strip tracker

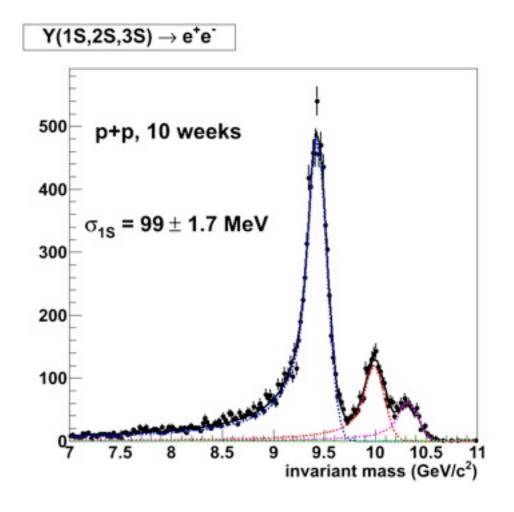
Outer radius 80 cm needed to meet momentum resolution spec Total thickness 2.6% + 6.7% = 9.3%

Revised MIE reference design - performance well studied in simulations









Questions/comments:

- Low cost
- Only two layers
- Significant dead areas in each layer

Scenario 3 - questions to be addressed by simulations

We need simulations with a realistic ladder geometry

Do these give similar performance to our cylinder-cell geometry simulations?

Realistic ladder geometry exists now in G4 for the outer Si tracker

Test tilted stereo strips as an alternative to pattern recognition layers

- Tilted strips exist in G4 ladder geometry
- Still need to implement stereo strips in tracking (covariance matrix in fitting)

Evaluate performance with reconfigured PHENIX pixels & realistic dead maps

Implement a model of LANL LDRD detector, evaluate performance

Evaluate performance with 3 pixel layers of ITS instead of PHENIX pixels

Summary

Can consider the inner tracker and outer tracker as separate building blocks, with different primary functions.

• They are connected by the need to obtain good overall track pattern recognition

A low mass outer tracker produces good Upsilon mass resolution and small radiative tails, regardless of whether we use Si or TPC technology.

I have considered three scenarios based on the choice of outer tracker, with several alternative inner tracker options for each scenario. For each scenario I have tried to outline what questions I think we should address using G4 simulations.

We should seriously consider how we want to balance mass resolution vs cost. If 100 MeV mass resolution is good enough, how much should we spend to do better? This applies to both Si and TPC options.

For sPHENIX I suggest that we consider all three of the scenarios outlined (and their variations 2a, 2b and 3a, 3b) to the point where we can make an initial comparison of cost, performance and technical risk.



Table 1.1: Geometrical parameters of the upgraded ITS.

	Inner Barrel Inner Layers			Outer Barrel			
				Middle Layers		Outer Layers	
	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4	Layer 5	Layer 6
Radial position (min.) (mm)	22.4	30.1	37.8	194.4	243.9	342.3	391.8
Radial position (max.) (mm)	26.7	34.6	42.1	197.7	247.0	345.4	394.9
Length (sensitive area) (mm)	271	271	271	843	843	1475	1475
Pseudo-rapidity coverage ^a	± 2.5	± 2.3	±2.0	±1.5	±1.4	±1.4	±1.3
Active area (cm ²)	421	562	702	10483	13104	32105	36 691
Pixel Chip dimensions (mm ²)				15×30			
Nr. Pixel Chips	108	144	180	2688	3360	8232	9408
Nr. Staves	12	16	20	24	30	42	48
Staves overlap in $r\phi$ (mm)	2.23	2.22	2.30	4.3	4.3	4.3	4.3
Gap between chips in z (µm)				100			
Chip dead area in $r\phi$ (mm)				2			
Pixel size (µm ²)	$(20-30)\times(20-30)$			$(20-50)\times(20-50)$			

^a The pseudorapidity coverage of the detector layers refers to tracks originating from a collision at the nominal interaction point (z = 0).